REMARKS

This is a full and timely response to the final Office Action of April 14, 2006. Reexamination, reconsideration, and allowance of the application and all presently pending claims are respectfully requested.

Upon entry of this paper, claims 1, 2, 7, 8, 10, and 23-40 are pending in this application. Claims 35 and 38 have been directly amended via the amendments set forth herein, and claim 40 is newly added. Further, claim 36 has been canceled without prejudice or disclaimer. It is believed that the foregoing amendments add no new matter to the present application.

Response to §112 Rejections

Claim 38 presently stands rejected under 35 U.S.C. §112, second paragraph, as allegedly being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claim 38 has been amended herein thereby mooting the 35 U.S.C. §112, second paragraph, rejection of this claim. Accordingly, Applicant respectfully requests that the 35 U.S.C. §112, second paragraph, rejection of claim 38 be withdrawn.

Response to §103 Rejections

In order for a claim to be properly rejected under 35 U.S.C. §103, the combined teachings of the prior art references must suggest all features of the claimed invention to one of ordinary skill in the art. See, *e.g.*, *In Re Dow Chemical Co.*, 837 F.2d 469, 5 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1988), and *In re Keller*, 642 F.2d 413, 208 U.S.P.Q. 871, 881 (C.C.P.A. 1981).

Claim 1

Claim 1 presently stands rejected under 35 U.S.C. §103 as allegedly being obvious over *Knowles* (U.S. Patent No. 6,446,107) in view of *Taewhan* ("Arithmetic Optimization using Carry-Save-Adders"). Claim 1 presently reads as follows:

> 1. An apparatus for performing addition of propagate, kill, and generate recoded numbers, said apparatus comprising:
>
> circuitry configured to receive at least a first operand, a second operand, and a carry-in bit, the first and second operands comprising respective first and second propagate, kill, and generate recoded number representations of respective first and second binary operands;
>
> a first carry-save adder configured to add said first operand and said second operand to generate a third propagate, kill, and generate recoded number representation and a carry-out bit; and
>
> a modified carry-save adder configured to receive the third propagate, kill, and generate recoded number representation from the first carry-save adder and the carry-in bit from the circuitry, add the separate propagate, kill, and generate bits of the third propagate, kill, and generate recoded number representation with the carry-in bit to generate a sum value and a carry value, wherein the circuitry provides the carry-out bit from the first carry-save adder at a first output and the carry value from the modified carry-save adder at a second output,
>
> wherein each of the propagate, kill, and generate recoded number representations has a respective kill bit, a respective propagate bit, and a respective generate bit that are indicative of a respective coded logical value having a plurality of bits, ***wherein the kill bit, if set, indicates that each of the bits of the respective coded logical value is not set***, wherein the propagate bit, if set, indicates that only one of the bits of the respective coded logical value is set, and wherein the generate bit, if set, indicates that each of the bits of the respective coded logical value is set. (Emphasis added).

Applicant respectfully asserts that the combination of *Knowles* and *Taewhan* fails to suggest at least the features of claim 1 highlighted hereinabove. Therefore, the 35 U.S.C. §103 rejection of claim 1 is improper and should be withdrawn.

In rejecting claim 1, it is asserted in the Office Action that *Knowles* discloses:

> "an apparatus (e.g. abstract and col. 9 line 59 – col. 10 line 10) for performing addition of propagate, kill, and generate recoded numbers... wherein the kill bit, if at a particular binary value (e.g. co. 10, lines 17-21), indicates that each of the bits of the respective coded logical value is not (set)..."

However, Applicant observes that there is nothing in the cited art to suggest that the alleged "kill bit," if set, indicates that each of the bits of the alleged "coded logical value" is not set. In this regard, the alleged "kill bit" is defined as a_i OR b_i. See column 9, line 67. Thus, if the alleged "kill bit" is low, as suggested in the Office Action, then it appears that bits a and b each have the same value (*i.e.*, low) as the alleged "kill bit," and, if the alleged "kill bit" is high, at least one of the bits a or b has the same value (*i.e.*, high) of the alleged "kill bit." However, claim 1 specifically requires the "kill bit," if set, to be ***different*** than each of the bits of the "respective coded logical value." In particular, claim 1 recites "wherein the kill bit, ***if set***, indicates that each of the bits of the respective coded logical value is ***not set***." (Emphasis added).

In responding to Applicant's arguments in the Amendment filed on February 2, 2006, it is asserted in the outstanding Office Action that:

> "Applicant's arguments filed 02/02/2006 have been fully considered but they are not persuasive.
>
> a. The applicant argues in pages 9-13 for all claims that the cited reference fails to disclose generally and particularly the kill bit, if set, indicates that each of the bits of the respective code logical value is not set as cited in the claim.
>
> The examiner respectfully submits that the cited reference clearly disclose the above feature as seen in Figures 2-3 wherein bar (k_1) is OR of a_1 and b_1, thus mathematically, k_1 is bar($a_1 + b_1$) or is bar(a_1) *bar(b_1) which indicates that each of the bits of respective code logical value of a_1 and b_1 is not set."

The foregoing Office Action allegations appear to be based on the fact that the value on the output connection of OR gate 61 is labeled "bar(K_1)" in Figure 2. Regardless of how this value is labeled, it does not constitute a "kill bit," as defined by claim 1. In this regard, the bit on the output connection of OR gate 61, regardless of the states of the input bits a_1 and b_1, is always the same as at least one of the input bits a_1 or b_1. In particular, the value on output connection of

OR gate 61 is a_1 OR b_1, and such a value cannot constitute a "kill bit," for at least the reasons set forth above.

Moreover, if the output value of OR gate 61 is referred to as "bar(K_1)," then a bit value "K_1" may indeed be defined as "bar($a_1 + b_1$)," as alleged in the Office Action. However, such a hypothetical bit value "K_1" does not appear to be generated by the circuitry of Figures 2 or 3 of *Knowles* nor by the alleged "apparatus" purportedly suggested by the combination of *Knowles* and *Taewhan*. In this regard, the output of OR gate 61 is not "bar($a_1 + b_1$)" but is instead $a_1 + b_1$. Further, there is nothing in the cited art to suggest that the hypothetical bit value "K_1" (*i.e.*, bar($a_1 + b_1$)) is generated by any other component of the alleged "apparatus." Thus, Applicant submits that the alleged "apparatus" is ***not*** configured to "generate" the alleged "kill bit" if the alleged "kill bit" is assumed to be equal to "bar($a_1 + b_1$)," as alleged in the Office Action. For at least the foregoing reasons, Applicant respectfully asserts that the Office Action fails to establish that the cited art teaches circuitry configured to "generate" PKG (propagate, kill and generate) recoded number representations that respectively have propagate, kill, and generate bits, "wherein the kill bit, if set, indicates that each of the bits of the respective coded logical value is not set," as described by claim 1.

In the Advisory Action of July 17, 2006, it is asserted that:

> "Continuation of 11. does NOT place the application in condition for allowance because: Throughout the argument pages 8-16, the applicant argued that the cited reference fails to disclose the kill bit, if set, indicates that each of the bits of the respective coded logical value is not set and only one of the kill, propagate, and generate bits of each possible propagate, kill, and generate recoded number representation can simultaneously be at the particular binary value. The examiner respectfully submits that the following table clearly expresses all the limitations cited above:

A_i	B_i	Kill	Bar(kill)	G	P
0	0	0	1	0	0
0	1	1	0	0	1
1	0	1	0	0	1
1	1	1	0	1	0"

Applicant agrees that Bar(kill) in the above table would constitute a "kill bit" that "if set, indicates that each of the bits of the respective coded logical value is not set." See columns A_i, B_i, and Bar(kill) of the above table. However, Applicant respectfully submits that a result pursuant to the Bar(kill) column of Table 1 does not appear to be generated by the circuitry of Figures 2 or 3 of *Knowles* nor by the alleged "apparatus" purportedly suggested by the combination of *Knowles* and *Taewhan*. In this regard, the output of OR gate 61 in Figure 2 is not Bar(kill), as defined in the above table, but is instead the OR of A_i and B_i. See Figure 2.

For at least the above reasons, Applicant respectfully asserts that the Office Action fails to establish a *prima facie* case of obviousness with respect to each feature of claim 1. Therefore, the 35 U.S.C. §103 rejection of claim 1 should be withdrawn.

Claims 2, 23-25, 27-29, 33, and 34

Claim 2 presently stands rejected in the Office Action under 35 U.S.C. §103 as allegedly obvious over *Knowles* in view *Taewhan* and in view of *Miller* (U.S. Patent No. 5,706,323). Further, claims 23-25, 27-29, 33, and 34 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly being anticipated by *Knowles* in view of *Taewhan*. Applicant submits that the pending dependent claims 2, 23-25, 27-29, 33, and 34 contain all features of their respective independent claim 1. Since claim 1 should be allowed, as argued hereinabove, pending dependent claims 2, 23-25, 27-29, 33, and 34 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 1.

For example, claim 33 recites "wherein only a respective one of the kill, propagate, and generate bits of each possible propagate, kill, and generate recoded number representation can

be set." Applicant respectfully asserts that such features are not suggested by the cited art. Accordingly, the 35 U.S.C. §103 rejection of claim 33 is improper and should be withdrawn, notwithstanding the allowability of independent claim 1.

In this regard, it is alleged in the Office Action that:

> "Re claim 33, Knowles further discloses in Figure 3 only one of the kill, propagate, and generate bits of each possible propagate, kill, and generate recoded number representation can simultaneously be at the particular binary value (e.g. col. 9 line 59- col. 10 line 10)."

Applicant respectfully traverses the Office Action assertion that the cited section of *Knowles* (*i.e.*, column 9, line 59, through column 10, line 10) suggests each feature of claim 33. In this regard, there is at least one possible state of the input a_i and b_i for which multiple ones of the alleged kill, propagate, and generate bits would be set according to the formulas specified at column 9, lines 64-66. Thus, there is at least one possible PKG recoded number representation in which multiple kill, propagate, and generate bits would be set, and the cited art, therefore, fails to suggest at least "wherein ***only*** a respective ***one*** of the kill, propagate, and generate bits ***of each possible*** propagate, kill, and generate recoded number representation can be set," as described by claim 33. (Emphasis added). Accordingly, the Office Action fails to establish a *prima facie* case of obviousness with respect to the features of claim 33.

Claim 7

Claim 7 presently stands rejected under 35 U.S.C. §103 as allegedly being obvious over *Knowles* in view of *Taewhan*. Claim 7 presently reads as follows:

> 7. A method for processing propagate, kill, and generate representations of respective first and second binary operands, comprising:
>
> receiving a carry-in value and a first and a second propagate, kill, and generate representation of respective first and second binary operands;
>
> generating a third propagate, kill, and generate representation and a carry-out value responsive to the first and second propagate, kill, and generate representations;

logically combining the third propagate, kill, and generate representation with the carry-in value to generate a sum value and a carry value; and

providing the carry-out value, the carry value, and the sum value as a result of the addition of the first and second propagate, kill, and generate representations,

wherein each of the propagate, kill, and generate recoded number representations has a respective kill bit, a respective propagate bit, and a respective generate bit that are indicative of a respective coded logical value having a plurality of bits, ***wherein the kill bit, if set, indicates that each of the bits of the respective coded logical value is not set***, wherein the propagate bit, if set, indicates that only one of the bits of the respective coded logical value is set, and wherein the generate bit, if set, indicates that each of the bits of the respective coded logical value is set. (Emphasis added).

For at least reasons similar to those set forth hereinabove in the arguments for allowance of claim 1, Applicant respectfully asserts that the cited art fails to suggest at least the features of claim 7 highlighted above. Accordingly, the 35 U.S.C. §103 rejection of claim 7 is improper and should be withdrawn.

Claims 8, 10, 30, 32, 37, and 38

Claims 8, 30, 32, 37, and 38 presently stand rejected in the Office Action under 35 U.S.C. §103 as allegedly obvious over *Knowles* in view of *Taewhan*. Further, claim 10 presently stands rejected in the Office Action under 35 U.S.C. §103 as allegedly being obvious over *Knowles* in view of *Taewhan* and in view of *Miller*. Applicant submits that the pending dependent claims 8, 10, 30, 32, 37, and 38 contain all features of their respective independent claim 7. Since claim 7 should be allowed, as argued hereinabove, pending dependent claims 8, 10, 30, 32, 37, and 38 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 7.

For example, claim 38 recites "wherein only a respective one of the kill, propagate, and generate bits of each possible propagate, kill, and generate recoded number representation is set." Applicant respectfully asserts that such features are not suggested by the cited art. Accordingly, the 35 U.S.C. §103 rejection of claim 38 is improper and should be withdrawn, notwithstanding the allowability of independent claim 7.

Claim 35

Claim 35 presently stands rejected under 35 U.S.C. §103 as allegedly being obvious over *Knowles* in view of *Taewhan*. Claim 35 presently reads as follows:

> 35. An apparatus for performing addition, said apparatus comprising:
> a first carry save adder configured to receive a first operand defining a first logical value encoded in propagate, kill, and generate (PKG) form such that the operand has a propagate bit, a generate bit, and a kill bit, the first carry save adder configured to receive a second operand defining a second logical value encoded in PKG form such that the second operand has a propagate bit, a generate bit, and a kill bit, ***the first carry save adder further configured to sum the first and second operands in PKG form to provide a first sum output in PKG form and a first carry bit without decoding the first and second operands from PKG form, the first sum output having a propagate bit, a generate bit, and a kill bit,***
> wherein the first carry bit and the propagate, generate, and kill bits of the first sum output collectively represent a summation of the first and second operands, wherein the first sum output represents a third logical value encoded in PKG form, wherein the third logical value has a plurality of bits, wherein the kill bit of the first sum output, if set, indicates that none of the bits of the third logical value are set, wherein the propagate bit of the first sum output, if set, indicates that only one of the bits of the third logical value is set, and wherein the generate bit of the first sum output, if set, indicates that each of the bits of the third logical value is set. (Emphasis added).

Applicant respectfully asserts that the combination of *Knowles* and *Taewhan* fails to suggest at least the features of claim 35 highlighted hereinabove. Therefore, the 35 U.S.C. §103 rejection of claim 35 is improper and should be withdrawn.

In this regard, it is alleged in the Office Action that Figure 3 of *Knowles* depicts circuitry that adds an operand in PKG form. However, the outputs of Figure 3 are sum and carry bits, which are not in PKG form. Thus, *Knowles* fails to suggest at least "the first carry save adder further configured to sum the first and second operands in PKG form to provide a first sum output ***in PKG form*** and a first carry bit without decoding the first and second operands from PKG form, ***the first sum output having a propagate bit, a generate bit, and a kill bit,***" as described by pending claim 35. Further, *Taewhan* fails to remedy the foregoing deficiency of *Knowles*.

For at least the above reasons, Applicant respectfully asserts that the cited art fails to suggest each feature of claim 35, as amended. Therefore, the 35 U.S.C. §103 rejection of claim 35 should be withdrawn.

Claims 39 and 40

Claim 39 presently stands rejected in the Office Action under 35 U.S.C. §103 as allegedly obvious over *Knowles* in view of *Taewhan*. Further, claim 40 has been newly added via the amendments set forth herein. Applicant submits that the pending dependent claims 39 and 40 contain all features of their respective independent claim 35. Since claim 35 should be allowed, as argued hereinabove, pending dependent claims 39 and 40 should be allowed as a matter of law for at least this reason. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Furthermore, these dependent claims recite patentably distinct features and/or combinations of features that make them allowable, notwithstanding the allowability of their base claim 35.

For example, claim 39 recites "wherein a single one of the kill, propagate, and generate bits is set by the circuitry regardless of the logical value defined by the operand." Applicant respectfully asserts that such features are not suggested by the cited art. Accordingly, the 35

U.S.C. §103 rejection of claim 39 is improper and should be withdrawn, notwithstanding the allowability of independent claim 35.

Allowable Subject Matter

Claims 26 and 31 have been indicated as allowable by the outstanding Office Action if such claims are rewritten to include the limitations of their respective base claims. For at least the reasons set forth hereinabove, Applicant submits that the respective base claims 1 and 7 are allowable and claims 26 and 31 are, therefore, allowable as a matter of law. *In re Fine*, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988). Accordingly, Applicant respectfully submits that claims 26 and 31 are allowable in their present form.

CONCLUSION

Applicant respectfully requests that all outstanding objections and rejections be withdrawn and that this application and all presently pending claims be allowed to issue. If the Examiner has any questions or comments regarding Applicant's response, the Examiner is encouraged to telephone Applicant's undersigned counsel.

Respectfully submitted,

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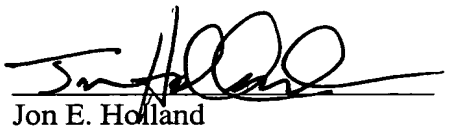
By: 

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